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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/033,188	10/25/2001	Mani Soma	02008.070001; AD-0318US	7329

22511 7590 08/05/2003

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EXAMINER	
DEB, ANJAN K	

ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 08/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

NC

Offic Action Summary	Application N .	Applicant(s)	
	10/033,188	SOMA ET AL.	
	Examiner	Art Unit	
	Anjan K Deb	2858	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2002 and 10 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6,7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 7 is objected to because of the following informalities: In claim 7, line 2, "riding" should be –rising--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagisawa et al. (US 6,528,982 B1).

Re claim 1, Yanagisawa et al. discloses a clock skew measuring apparatus for measuring a clock skew for measuring a clock skew between a plurality of clock signals (101) to be measured in a device under test comprising, clock skew estimator (103,104,106,111)) receiving a reference signal (102) input to device under test (10), and obtaining said clock skew between plurality of clock signals by measuring a timing difference measured by counter (105) between a received reference signal (102) and each of the plurality of clock signals to be measured (101).

Yanagisawa et al. did not expressly disclose a clock signal selecting element selecting clock signals to be measured one by one.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Yanagisawa et al. by adding a clock signal selecting element because comparison pulse generator (103) disclosed by Yanagisawa et al. performs comparison of one clock signal at a time (Fig. 2).

4. Claims 1-7, 13-14, 17-24, 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (US 6,522,122 B2).

Re claims 1,17-19 Watanabe et al. discloses (Fig. 5) a clock skew measuring apparatus and method for measuring a clock skew (jitter) between a plurality of clock signals (23) to be measured in a device under test (11) comprising a SAMPLING CIRCUIT (14)(Fig. 14) operable to receive plurality of clock signals to be measured, and to output plurality of clock signals to be measured by sampling (SAMPLING CIRCUIT (14)) plurality of clock signals (23) to be measured, a clock skew estimator (46) operable to receive a reference signal (31,32) input to device under test (11), and obtaining clock skew between plurality of clock signals to be measured by measuring a timing difference (S2)(Fig. 13) between received reference signal (31,32)(CHARACTERISTIC VALUE: Fig. 13) and each clock signal(23)(READ-IN DATA: Fig. 13). Deviation (S2) of the output of sampling circuit from one of rise-up and fall characteristics of the output from a waveform formatter (see claim 1) is broadly interpreted as measuring a timing difference.

Watanabe et al. did not expressly disclose a clock signal selecting element selecting clock signals to be measured one by one.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Watanabe et al. by adding clock signal selecting element required for sampling circuit (14 see Fig. 14) disclosed by Watanabe et al.

Re claim 2, Watanabe et al. did not expressly disclose buffer but a buffer would have been obvious for holding clock signals so that they can be sampled by sampling circuit 14.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Watanabe et al. by adding buffer for holding clock signals for sampling by a sampling circuit.

Re claims 3-4, 20-21 Watanabe et al. discloses determining a deterministic component (average value: S5) and random component (S6) (Fig. 13).

Re claims 5-7, 22-24, 30, Watanabe et al. discloses calculating clock skew by determining timing error from the deviation of the output of sampling circuit from rise-up and fall characteristics of the output from a waveform formatter (see claim 1) including calculating plurality of timing difference between read-in data and characteristic value S2, and obtaining mean value (S5) for calculating skew (Fig. 13).

Re claim 13, Watanabe et al. discloses A/D converter (24)(Fig. 14).

Re claim 14, 31 Watanabe et al. discloses removing amplitude modulation to extract phase modulation component as shown in Fig. 9C.

5. Claims 8-12, 15-16, 25-29, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (US 6,522,122 B2) in view of Jenq et al. (US 4,896,271).

Re claims 8,25 Watanabe et al. discloses an instantaneous phase estimator (phase detector 33) but did not expressly disclose the details of phase estimator.

Watanabe et al. did not expressly disclose an analytic transformer for obtaining an estimate of phase.

Jenq et al. (US 4,896,271) disclose an analytic transformer (51) for obtaining an estimate of phase by generating a third data sequence (S3) for obtaining an initial phase angle θ_k ($S3_0$) as shown in Fig. 4A.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Watanabe et al. by adding an analytic transformer disclosed by Jenq et al. for obtaining an initial phase angle.

Re claim 9, Watanabe et al. did not expressly disclose linear trend remover for obtaining a value of instantaneous phase noise.

Jenq et al. (US 4,896,271) disclose linear trend y_k (Fig. 6) remover ($s4_k = y_k - s3_k$) for obtaining a value of instantaneous phase noise (jitter) $s4_k$ as shown in Fig. 7.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Watanabe et al. by adding linear trend remover disclosed by Jenq et al. so that a deterministic component is removed for obtaining phase noise.

Re claims 10-11, Watanabe et al. did not expressly disclose Hilbert transformer.

Jenq et al. (US 4,896,271) disclose performing time domain to frequency domain transformation by Fourier Transformer H(w).

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Watanabe et al. by adding Hilbert Transformation for obtaining amplitude and phase of clock signal because Jenq et al disclosed obtaining amplitude and phase of clock signal by performing Fourier Transformation H(w).

Re claims 12, 27-29 Watanabe et al. did not expressly disclose a window function.

Jenq et al. (US 4,896,271) disclose window function (column 4, lines 59-60) for selecting and extracting a portion of the data by Fourier Transformation (column 4 lines 61-68) for obtaining band limited time domain time signal $S2_k$ (column 5 lines (19-36).

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Watanabe et al. by adding window function disclosed by Jenq et al. for obtaining band limited time domain time signal.

Re claim 26, Watanabe et al. discloses removing amplitude modulation to extract phase modulation component as shown in Fig. 9C.

Re claim 15, Watanabe et al. and Jenq et al. did not expressly disclose variable bandwidth analytic transformer for phase estimation.

Jenq et al. (US 4,896,271) disclose an analytic transformer (51) for phase estimation comprising digital filter (14-18).

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Watanabe et al. and Jenq et al. by adding digital filters disclosed by Jenq et al. having variable bandwidth for achieving a desired frequency response.

Re claims 16,32 Jenq et al. (US 4,896,271) discloses removing low frequency (DC) component (column 3 lines 1-12) for estimating a second data sequence.

At the time of the invention it would have been obvious for one of ordinary skill in the art to modify Watanabe et al. by adding removing low frequency (DC) component disclosed by Jenq et al for estimating a second data sequence for phase estimation.

Pertinent Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kazami (US 5,578,938) discloses method and apparatus for measuring clock skew comprising applying test signal at pin 18 connected to I/O buffer 17, and detecting skew by the output of XOR gate output pin 16 (Fig. 4)

Huffman (US 4,412,299) discloses method and apparatus for measuring clock skew by determining deviation of phase difference of clock signal between transitions X_i from the mean time X between transitions ($X_i - X$) (see Fig. 6).

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Anjan K. Deb whose telephone number is (703) 308-2941. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le, can be reached at (703)-308-0750.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone numbers are (703)-308-0956 and (703)-305-4900.

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7/30/03

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